US 20080237585A1

(19) **United States**

(12) **Patent Application Publication**

(10) **Pub. No.: US 2008/0237585 A1**

(43) **Pub. Date: Oct. 2, 2008**

Kim

(54) **FLAT PANEL DISPLAY DEVICE AND METHOD OF FABRICATING THE SAME**

(76) Inventor: **Jong-Yun Kim**, Suwon-si (KR)

Correspondence Address:
KNOBBE MARTENS OLSON & BEAR LLP
2040 MAIN STREET, FOURTEENTH FLOOR
IRVINE, CA 92614 (US)

(21) Appl. No.: **12/079,720**

(22) Filed: **Mar. 28, 2008**

(30) **Foreign Application Priority Data**

Mar. 28, 2007 (KR) 10-2007-0030478

Publication Classification

(51) **Int. Cl.**
H01L 51/00 (2006.01)
H01L 21/02 (2006.01)

(52) **U.S. Cl.** **257/40**; 438/29; 257/E51.018; 257/E21.002

(57) **ABSTRACT**

A flat panel display device including a first region having an organic light emitting diode and a thin film transistor and a second region having a capacitor is disclosed. The capacitor comprises first, second, and third electrodes, where the area of a third capacitor electrode is reduced, thereby ensuring a distance between a first power voltage line and the third capacitor electrode. The total area of the capacitor is compensated by increasing the area of the first capacitor electrode. Thus, the area of the third capacitor electrode is reduced while the total capacitance of the capacitor is maintained, thereby preventing a dark spot caused by a short circuit between the first power voltage line and the third capacitor electrode.

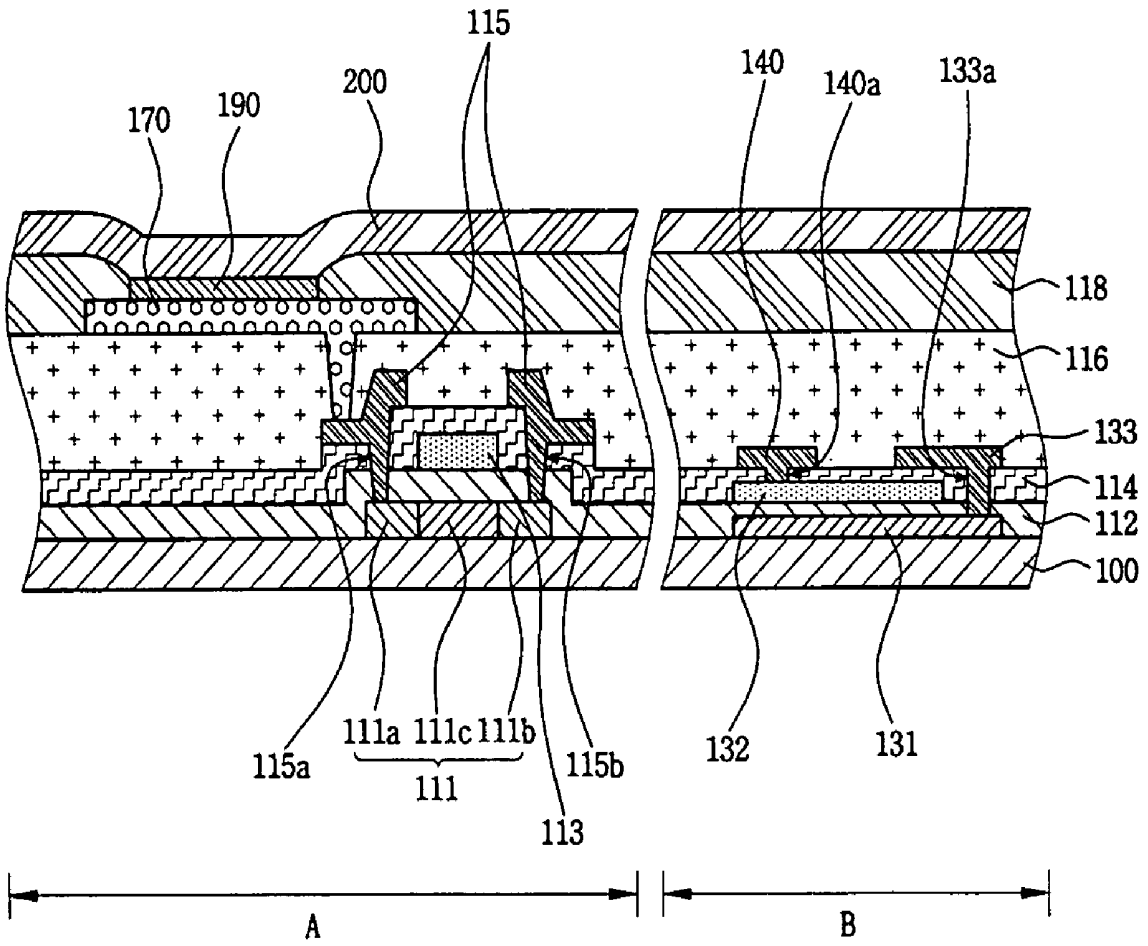


FIG. 1

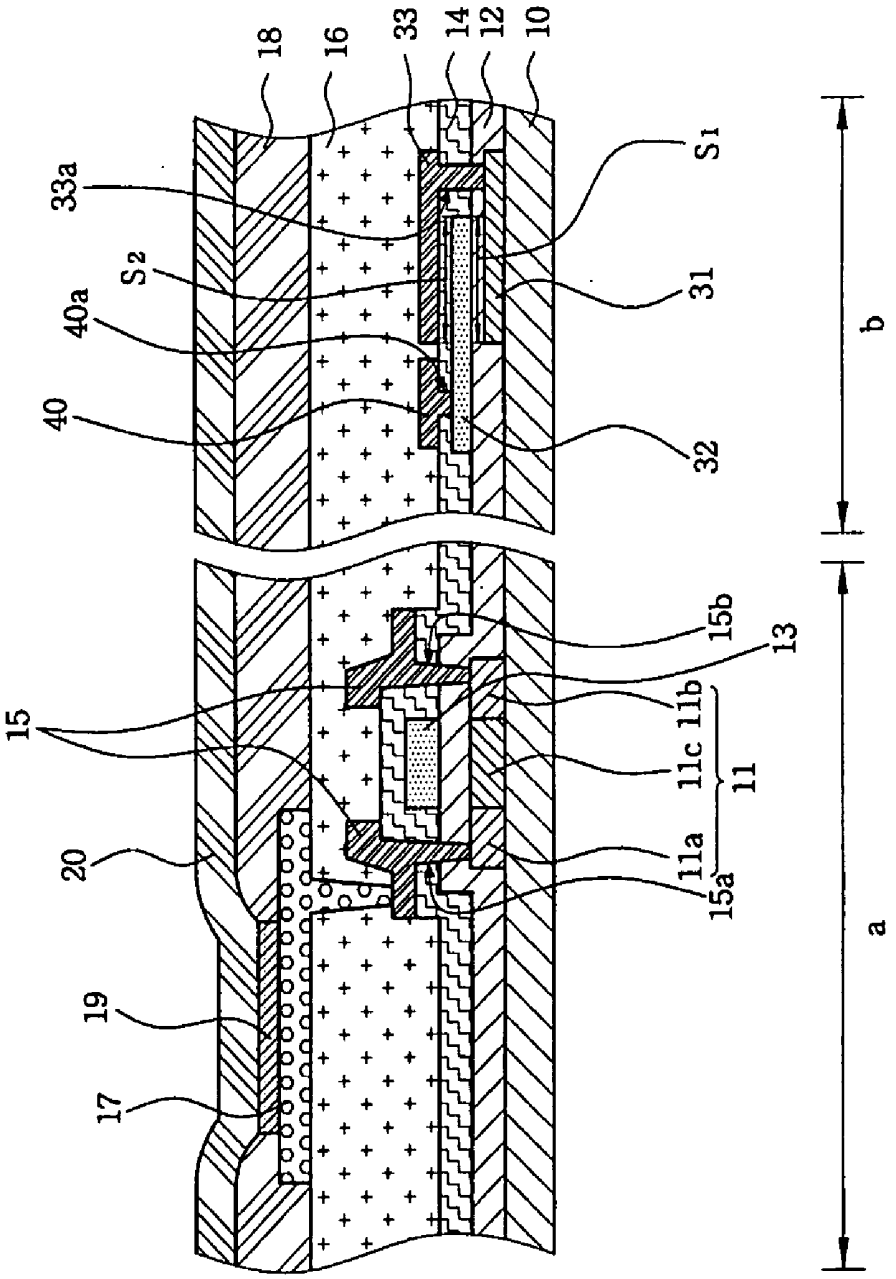

18
16
33
14
12
10
33a
S2
40a
40
S1
31
32
b
15b
13
15
11b
11c
11
11a
15a
20
19
17
a

FIG. 2A

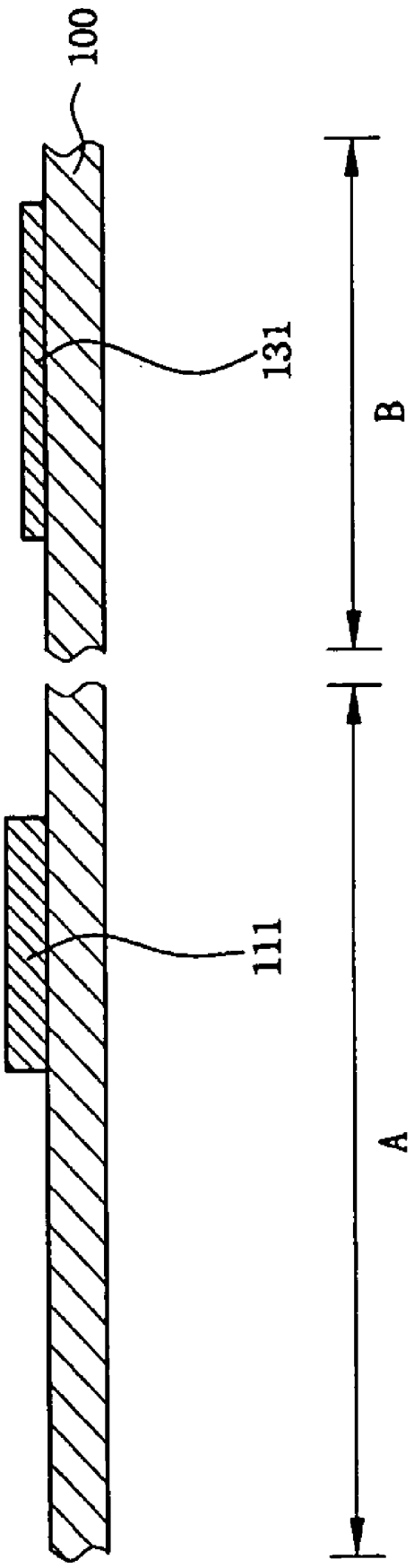


FIG. 2B

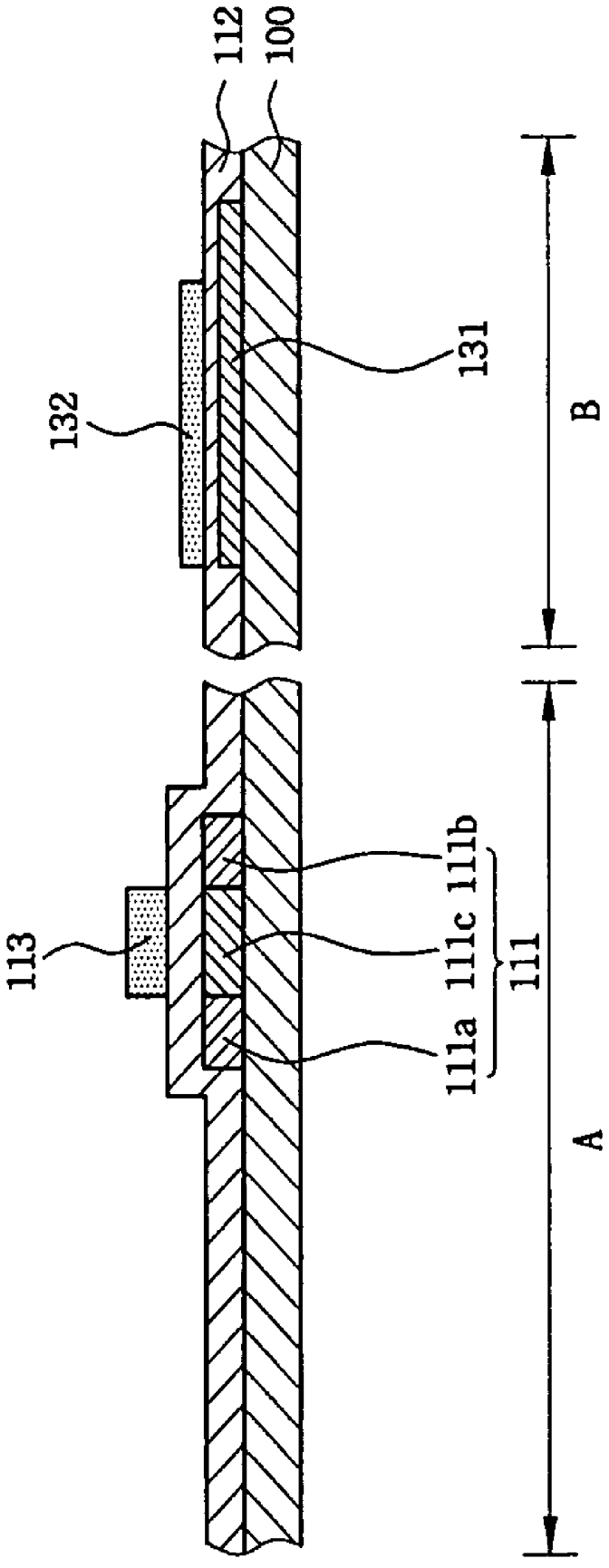


FIG. 2C

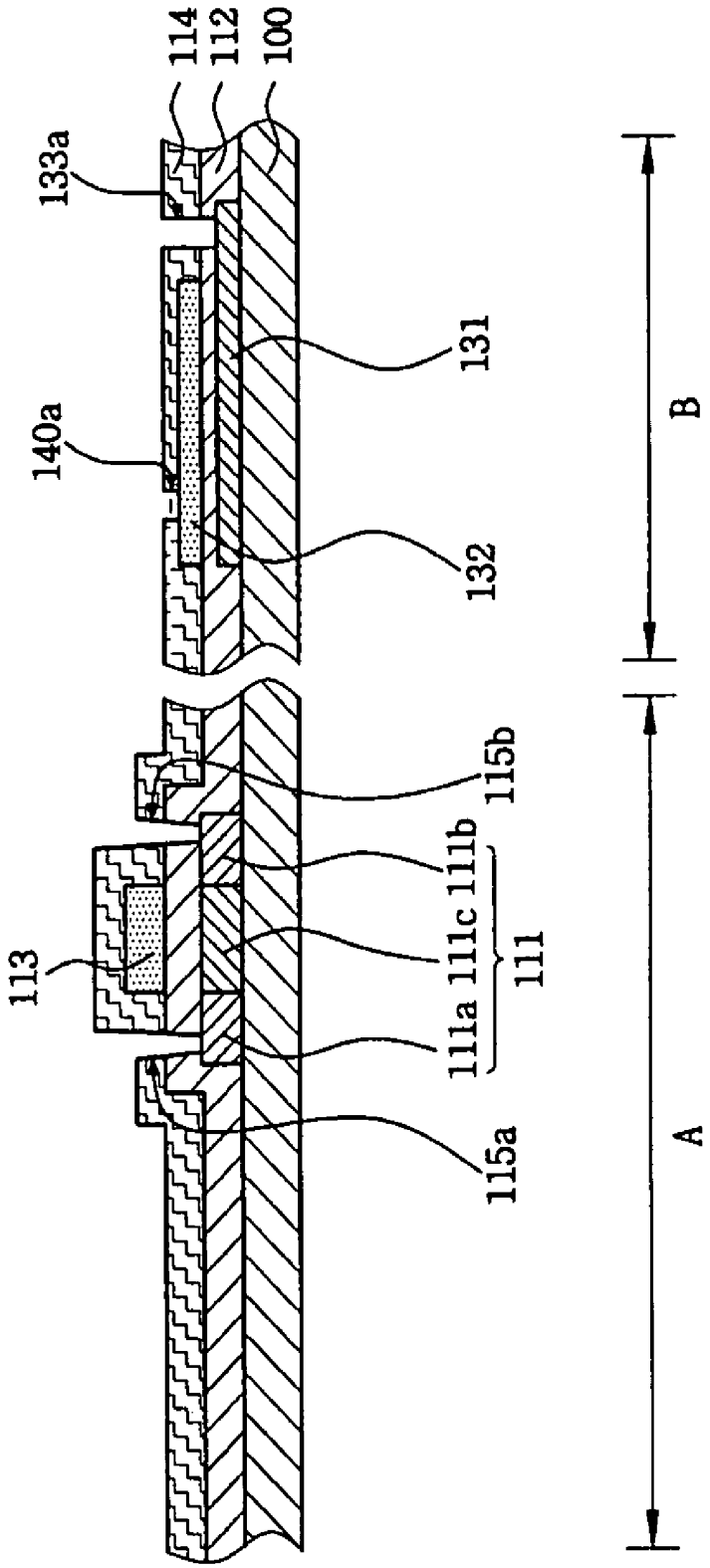

114
112
100
133a
131
140a
132
B
115b
111b
113
111c
111
111a
115a
A

FIG. 2D

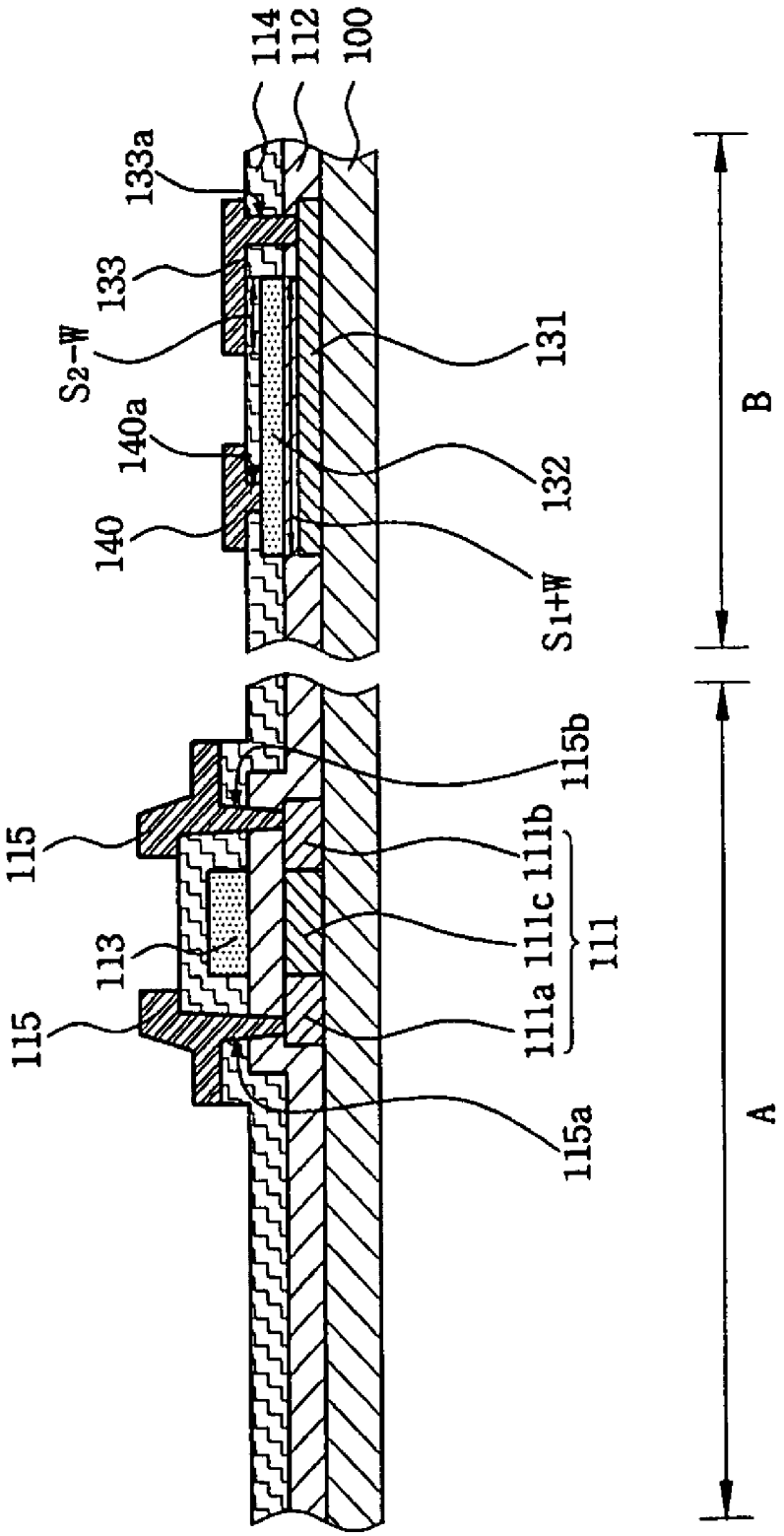
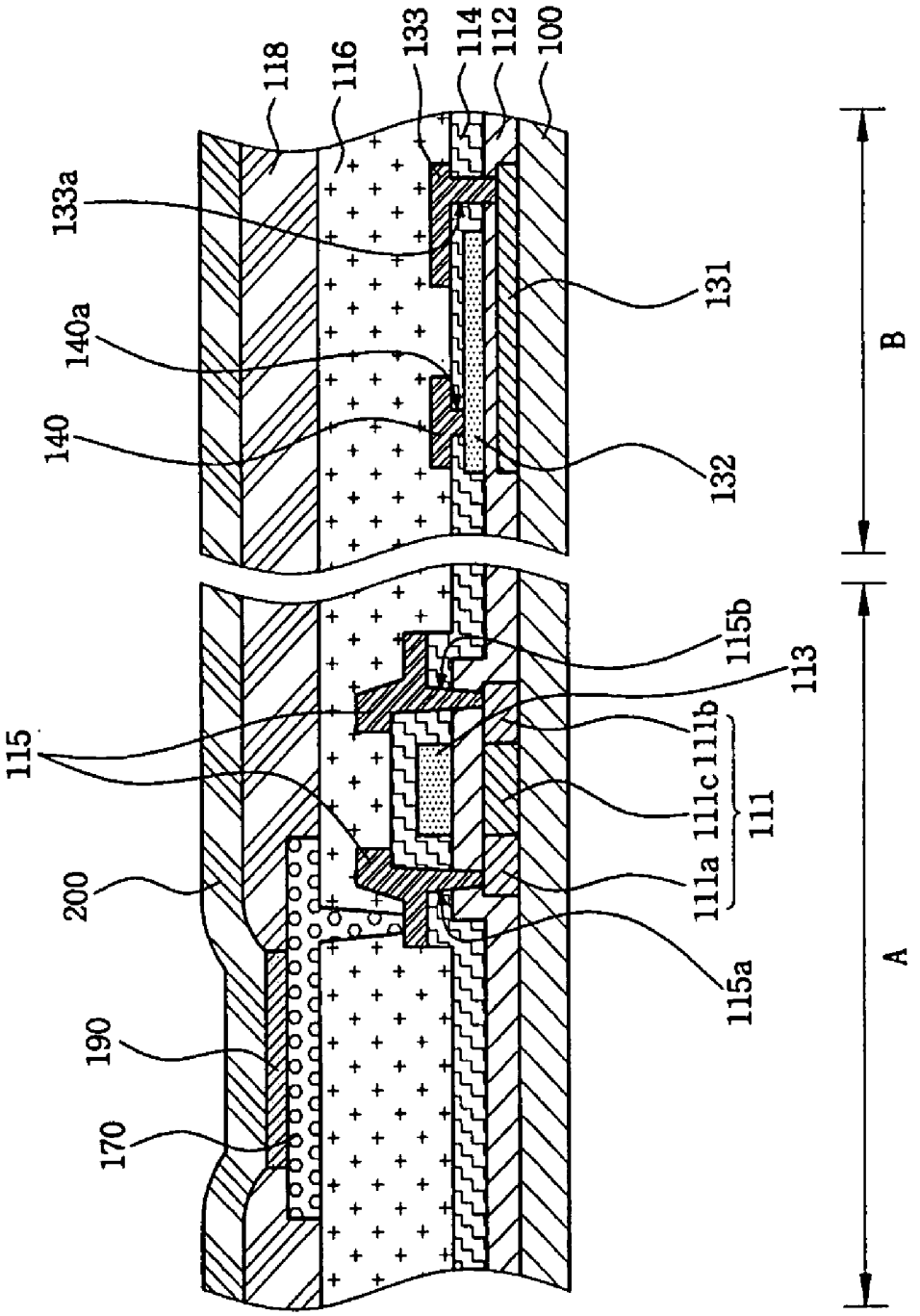

114
112
100
133a
133
S2-W
131
140a
132
140
S1+W
B
115b
115
111b
111c
111
113
111a
115
115a
A

FIG. 2E


118
116
133
114
112
100
133a
131
140a
140
132
B
115b
113
115
111b
111c
111
111a
200
115a
190
170
A

FLAT PANEL DISPLAY DEVICE AND METHOD OF FABRICATING THE SAME

CROSS-REFERENCE TO RELATED APPLICATION

[0001] This application claims the benefit of Korean Patent Application No. 2007-30478, filed Mar. 28, 2007, the disclosure of which is hereby incorporated herein by reference in its entirety.

BACKGROUND OF THE INVENTION

[0002] 1. Field

[0003] The field relates to a flat panel display device and a method of fabricating the same, and more particularly, to a flat panel display device including a capacitor having first and second capacitors, wherein the capacitor has a first capacitor electrode and a third capacitor electrode which are different in area.

[0004] 2. Description of Related Technology

[0005] Generally, an organic light emitting diode (OLED) display device, one kind of a flat panel display device, is a self-emissive display device which electrically excites an emissive organic compound so as to emit light, and is classified as a passive-matrix device or an active-matrix device based on its driving mechanism.

[0006] The active-matrix OLED display device includes a thin film transistor, and is suitable for large-sized display device because of less power consumption than the passive-matrix OLED display device.

[0007] This active-matrix OLED display device includes thin film transistors and capacitors in a compensation circuit.

[0008] FIG. **1** is a cross-sectional view of a conventional OLED display device.

[0009] Referring to FIG. **1**, an amorphous silicon layer is formed on a substrate **10** including a first region a in which an organic light emitting diode (OLED) and a thin film transistor are formed and a second region b in which a capacitor is formed, and then crystallized to form a polycrystalline silicon layer.

[0010] After crystallization into the polycrystalline silicon layer, the polycrystalline silicon layer is patterned so as to form a semiconductor layer **11** in the first region a, and form a first capacitor electrode **31** in the second region b.

[0011] Then, a gate insulating layer **12** is formed on the entire surface of the substrate, and a gate metal layer is deposited on the gate insulating layer **12**. The gate metal layer is patterned so as to form a gate electrode **13** corresponding to a certain region of the semiconductor layer **11** in the first region a.

[0012] The gate metal layer is patterned so as to form a second capacitor electrode **32** corresponding to a certain region of the first capacitor electrode **31** on the gate insulating layer **12** in the second region b, while forming the gate electrode **13**.

[0013] Subsequently, n- or p-type impurity ions are injected into the semiconductor layer **11**, thereby forming source and drain regions **11***a* and **11***b*. Here, a channel region **11***c* is formed between the source and drain regions **11***a* and **11***b* of the semiconductor layer **11**.

[0014] After forming an interlayer insulating layer **14** on the entire surface of the substrate, the interlayer insulating layer **14** and the gate insulating layer **12** are etched in the first region a, thereby forming first and second contact holes **15***a* and **15***b* which partially expose the source and drain regions **11***a* and **11***b* of the semiconductor layer **11**, respectively.

[0015] A third contact hole **40***a* partially exposing the second capacitor electrode **32** and a fourth contact hole **33***a* partially exposing the first capacitor electrode **31** are formed in the second regions b.

[0016] Then, source and drain metal layers are deposited on the interlayer insulating layer **14** and are then patterned in a certain shape in the first region a so as to form source and drain electrodes **15** which are connected with the source and drain regions **11***a* and **11***b* of the semiconductor layer **11** through the first and second contact holes **15***a* and **15***b*, respectively.

[0017] Also, a first power voltage line **40** connected with the second capacitor electrode **32** through a third contact hole **40***a*, and a third capacitor electrode **33** connected with the first capacitor electrode **31** through a fourth contact hole **33***b* are formed in the second region b.

[0018] The first capacitor electrode **31** and the second capacitor electrode **32** constitute a first capacitor. Here, the first capacitor electrode **31** is a lower electrode of the first capacitor, and the second capacitor electrode **32** is an upper electrode of the first capacitor. Also, the second capacitor electrode **32** and the third capacitor electrode **33** constitute a second capacitor, wherein the second capacitor electrode **32** is a lower electrode of the second capacitor, and the third capacitor electrode **33** is an upper electrode of the second capacitor.

[0019] Here, the first capacitor electrode **31** and the third capacitor electrode **33** have the same area so that an area S2 corresponding to the third capacitor electrode **33** overlap of the second capacitor electrode **32** is equal to an area SI corresponding to the second capacitor electrode **32** overlap of the first capacitor electrode **31**.

[0020] Thus, when the permittivity and distance between the first capacitor and the second capacitor are equal, the capacitances of the capacitors are also equal.

[0021] A passivation layer **16** is formed on the entire surface of the substrate, and a planarization layer (not illustrated) may be formed of an organic material to reduce a step height on the substrate.

[0022] Here, a pixel electrode **17** is formed in the first region a, which is electrically connected with one of the source and drain electrodes **15** through a via hole passing through the passivation layer **16** or the planarization layer.

[0023] Subsequently, a pixel defining layer **18** including an opening partially exposing the pixel electrode **17** is formed. An organic layer **19** including an organic emitting layer is formed on the pixel electrode **17** exposed by the opening, and a counter electrode **20** is formed on the entire surface of the substrate, and thus the OLED display device may be completed.

[0024] However, the distance between the third capacitor electrode **33** and the first power voltage line **40** is relatively small, which is within 5 μm, because the area of the third capacitor electrode **33** has to be large to increase the capacitance of the capacitor.

[0025] The small distance between interconnections may cause a short circuit between the third capacitor electrode **33** and the first power voltage line **40** in the patterning process.

[0026] As a result, the capacitor is short-circuited, so that the voltage between the gate and the source electrode of the

thin film transistor is 0 and no current flows, and thus a dark spot occurs in the OLED display device.

SUMMARY OF CERTAIN INVENTIVE ASPECTS

[0027] One aspect is a flat panel display device, including a substrate with a first region on which an organic light emitting diode and a thin film transistor are formed and a second region on which a capacitor is formed. The device also includes a semiconductor layer with source and drain regions on the first region, a first capacitor electrode formed on the second region, a gate insulating layer formed on the substrate, a gate electrode formed on the first region on the gate insulating layer, a second capacitor electrode formed on the second region, an interlayer insulating layer formed on the substrate, source and drain electrodes formed on the first region on the interlayer insulating layer and connected with the semiconductor layer through first and second contact holes. The device also includes a first power voltage line formed on the second region connected with the second capacitor electrode through a third contact hole, and a third capacitor electrode formed on the second region connected with the first capacitor electrode through a fourth contact hole, and having a different area from the first capacitor electrode.

[0028] Another aspect is a method of fabricating a flat panel display device. The method includes providing a substrate including a first region on which an organic light emitting diode and a thin film transistor are formed and a second region on which a capacitor is formed. The method also includes forming a semiconductor layer on the first region, forming a first capacitor electrode on the second region, forming a gate insulating layer on the substrate, forming a gate electrode on the first region on the gate insulating layer, forming a second capacitor electrode on the second region on the gate insulating layer, and injecting a dopant into the semiconductor layer and forming source and drain regions. The method also includes forming an interlayer insulating layer on the substrate, forming first and second contact holes respectively exposing the source and drain regions on the interlayer insulating layer, forming third and fourth contact holes respectively exposing the first capacitor electrode and the second capacitor electrode, forming source and drain electrodes connected with the source and drain regions through the first and second contact holes on the first region on the interlayer insulating layer, forming a first power voltage line connected with the second capacitor electrode through the third contact hole, and forming a third capacitor electrode connected with the first capacitor electrode through the fourth contact hole and having a different area from the first capacitor electrode on the second region on the interlayer insulating layer.

BRIEF DESCRIPTION OF THE DRAWINGS

[0029] The above and other features will be described in reference to certain embodiments thereof with reference to the attached drawings in which:

[0030] FIG. **1** is a cross-sectional view of a conventional organic light emitting diode (OLED) display device; and

[0031] FIGS. **2**A to **2**E are cross-sectional views illustrating a method of fabricating an OLED display device.

DETAILED DESCRIPTION OF CERTAIN INVENTIVE EMBODIMENTS

[0032] Certain embodiments will now be described more fully hereinafter with reference to the accompanying drawings.

[0033] FIGS. **2**A to **2**E are cross-sectional views illustrating an innovative method of fabricating an OLED display device.

[0034] First, referring to FIG. **2**A, a buffer layer (not illustrated) is formed to prevent the diffusion of moisture or impurities, or to control thermal transmission in the crystallization on a substrate **100**.

[0035] An amorphous silicon layer is formed on the buffer layer, and then crystallized to form a polycrystalline silicon layer. The crystallization of the amorphous silicon layer may be performed by excimer laser annealing (ELA), sequential lateral solidification (SLS), metal induced crystallization (MIC) or metal induced laser crystallization (MILC). The polycrystalline silicon layer includes a first region A in which an organic light emitting diode (OLED) and a thin film transistor are formed and a second region B in which a capacitor (Cst) is formed.

[0036] The polycrystalline silicon layer is patterned in a certain shape, so as to form a first capacitor electrode **131** in the second region B while forming a semiconductor layer **111** in the first region A.

[0037] Referring to FIG. **2**B, a gate insulating layer **112** is formed on the entire surface of the substrate, and a gate metal layer, which may, for example, be formed of one of aluminum (Al), an Al alloy, molybdenum (Mo) and a Mo alloy, is deposited on the gate insulating layer **112**.

[0038] Then, the gate metal layer is patterned so as to form a gate electrode **113** corresponding to a certain region of the semiconductor layer **111** in the first region A. While forming the gate electrode **113**, a second capacitor electrode **132** corresponding to a certain region of the first capacitor electrode **131** is formed by patterning the gate metal layer on the gate insulating layer **112** in the second region B.

[0039] An n- or p-type dopant is injected into the semiconductor layer **111** using the gate electrode **113** as a mask so as to form source and drain regions **111***a* and **111***b*.

[0040] Beneath the gate electrode **113**, a channel region **111***c* is formed between the source and drain regions **111***a* and **111***b* of the semiconductor layer **111**.

[0041] Referring to FIG. **2**C, an interlayer insulating layer **114** is formed on the entire surface of the substrate.

[0042] Then, the interlayer insulating layer **114** and the gate insulating layer **112** are etched to respectively form first and second contact holes **115***a* and **115***b* at least partially exposing the source and drain regions **111***a* and **111***b* of the semiconductor layer **111** in the first region A. A third contact hole **140***a* partially exposing the second capacitor electrode **132** and a fourth contact hole **133***a* partially exposing the first capacitor electrode **131** are formed in the second region B.

[0043] The buffer layer (not illustrated), the gate insulating layer **112** and the interlayer insulating layer **114** may be formed of SiO_2, SiNx, or a multi-layer thereof.

[0044] Referring to FIG. **2**D, source and drain metal layers formed, for example, of one of Al, an Al alloy, Mo and a Mo alloy is deposited on the interlayer insulating layer **114**.

[0045] The source and drain metal layers are patterned in a certain shape to form source and drain electrodes **115**, which are respectively connected with the source and drain regions **111***a* and **111***b* of the semiconductor layer **111** through the first and second contact holes **115***a* and **115***b* in the first region A.

[0046] A first power voltage line **140** connected with the second capacitor electrode **132** through the third contact hole **140***a*, and a third capacitor electrode **133** connected with the

first capacitor electrode **131** through the fourth contact hole **133***a* are formed in the second region B.

[0047] Here, the first capacitor electrode **131** and the second capacitor electrode **132** constitute a first capacitor (Cst**1**), wherein the first capacitor electrode **131** is a lower electrode of the first capacitor (Cst**1**), and the second capacitor electrode **132** is an upper electrode of the first capacitor (Cst**1**). The second capacitor electrode **132** and the third capacitor electrode **133** constitute a second capacitor (Cst**2**), wherein the second capacitor electrode **132** is a lower electrode of the second capacitor (Cst**2**), and the third capacitor electrode **133** is an upper electrode of the second capacitor (Cst**2**). As a result, the first and second capacitors form a capacitor (Cst).

[0048] The first capacitor electrode **131** and the third capacitor electrode **133** are different in area. To preserve the total capacitance and increase the spacing between the third capacitor electrode **133**, the area of the first capacitor electrode **131** is larger than the area of the third capacitor electrode **133**.

[0049] Here, the capacitance of the capacitor between two electrodes may be expressed by the following equation.

$$C=\epsilon(S/d)$$

[0050] Here, ϵ represents permittivity, S represents area between the two electrodes, and d represents a distance between two electrodes.

[0051] When the area of the third capacitor electrode **133**, i.e., the upper electrode of the second capacitor (Cst**2**), is smaller than a certain area S**2**, the corresponding area between the third capacitor electrode **133** and the second capacitor electrode **132** is smaller by a variation W in area of the capacitor. As a result, the capacitance of the second capacitor (Cst**2**) is reduced by $\epsilon_2 W/d_2$, that is $Cst2=\epsilon_2 S_2/d_2-\epsilon_2 W/d_2$.

[0052] Similarly, when the area of the first capacitor electrode **131**, i.e., the lower electrode of the first capacitor (Cst**1**), is larger than a certain area S_1(=S**2**), the corresponding area between the first capacitor electrode **131** and the second capacitor electrode **132** is larger by W. Accordingly, the capacitance of the first capacitor (Cst**1**) is increased by $\epsilon_1 W/d_1$, that is $Cst1=\epsilon_1 S_1/d_1+\epsilon_1 W/d_1$.

[0053] As a result, the first capacitor electrode **131** corresponding to the second capacitor electrode **132** and the third capacitor electrode **133** have an area difference of W×2.

[0054] Therefore, capacitance of the capacitor (Cst) is the same as the capacitance of the capacitor if the areas of the third capacitor electrode **133** and the first capacitor electrode **131** were both the same, that is $Cst=Cst1+Cst2=\epsilon_1 S_1/d_1+\epsilon_1 W/d_1+\epsilon_2 S_2/d_2-\epsilon_2 W/d_2$. When the permittivity and distance between the first capacitor (Cst**1**) and the second capacitor (Cst**2**) are equal, $\epsilon_1 W/d_1=\epsilon_2 W/d_2$, and $Cst=\epsilon_1 S_1/d_1+\epsilon_2 S_2/d_2$. Therefore, when the permittivity and distance between the first capacitor (Cst**1**) and the second capacitor (Cst**2**) are equal, the capacitance Cst is equal to the capacitance if the area of the first capacitor Cst**1** and the area of second capacitor Cst**2** were both the same.

[0055] Accordingly, in the above-described manner, while maintaining the same total capacitance, the distance between the first power voltage line **140** and the third capacitor electrode **133** may be increased, thereby preventing a short circuit between the first power voltage line **140** and the third capacitor electrode **133** which may occur in fabrication.

[0056] Then, referring to FIG. **2**E, a passivation layer **116**, formed, for example, of SiO_2, SiNx or a multi-layer thereof is formed on the entire surface of the substrate, and a planarization layer (not illustrated) formed, for example, of an organic material may be formed to reduce a step height on the substrate.

[0057] Here, a pixel electrode **170** electrically connected with one of the source and drain electrodes **115** through a via hole passing through the passivation layer **116** or the planarization layer is formed in the first region A. The pixel electrode **170** may have a stacked structure of a transparent electrode such as indium tin oxide (ITO) or indium zinc oxide (IZO) and a reflective electrode formed of one selected from the group consisting of Pt, Au, Ir, Cr, Mg, Ag, Al and an alloy thereof.

[0058] A pixel defining layer **118** including an opening exposing a partial region of the pixel electrode **170** is formed on the entire surface of the substrate. The pixel defining layer **118** may be formed, for example, of one selected from the group consisting of benzocyclobutene (BCB), an acryl-based polymer and polyimide.

[0059] Then, an organic layer **190** including an organic emitting layer may be formed on the pixel electrode **170** exposed by the opening, and a counter electrode **200** may be formed on the entire surface of the substrate.

[0060] Consequently, according to a flat panel display device and a method of fabricating the same, it is possible to ensure the distance between a first power voltage line and a third capacitor electrode by reducing the area of the third capacitor electrode of a capacitor (Cst). At the same time, the capacitance of the capacitor (Cst) according to the reduction in area of the third capacitor electrode may be compensated by increasing the area of a first capacitor electrode.

[0061] Thus, a dark spot caused by a short circuit between the first power voltage line and the third capacitor electrode may be prevented while retaining the capacitance of the capacitor (Cst) and decreasing the area of the third capacitor electrode.

[0062] Although the certain embodiments been described with reference to the figures, it will be understood by those skilled in the art that a variety of modifications and variations may be made to the embodiments without departing from the spirit or scope of the present invention.

What is claimed is:

1. A flat panel display device, comprising:

a substrate including a first region on which an organic light emitting diode and a thin film transistor are formed and a second region on which a capacitor is formed;

a semiconductor layer including source and drain regions on the first region;

a first capacitor electrode formed on the second region;

a gate insulating layer formed on the substrate;

a gate electrode formed on the first region on the gate insulating layer;

a second capacitor electrode formed on the second region;

an interlayer insulating layer formed on the substrate;

source and drain electrodes formed on the first region on the interlayer insulating layer and connected with the semiconductor layer through first and second contact holes;

a first power voltage line formed on the second region connected with the second capacitor electrode through a third contact hole; and

a third capacitor electrode formed on the second region connected with the first capacitor electrode through a fourth contact hole, and having a different area from the first capacitor electrode.

2. The display device according to claim **1**, wherein the first capacitor electrode is formed from the same material as the semiconductor layer.

3. The display device according to claim **1**, wherein the second capacitor electrode is formed from the same material as the gate electrode.

4. The display device according to claim **1**, wherein the first power voltage line is formed from the same material as the source and drain electrodes.

5. The display device according to claim **1**, wherein the third capacitor electrode is formed from the same material as the source and drain electrodes.

6. The display device according to claim **1**, wherein the first capacitor electrode is formed in substantially the same layer as the semiconductor layer.

7. The display device according to claim **1**, wherein the second capacitor electrode is formed in substantially the same layer as the gate electrode.

8. The display device according to claim **1**, wherein the first power voltage line is formed in substantially the same layer as the source and drain electrodes.

9. The display device according to claim **1**, wherein the third capacitor electrode is formed in substantially the same layer as the source and drain electrodes.

10. The display device according to claim **1**, wherein the first capacitor electrode corresponding to the second capacitor electrode and the third capacitor electrode have an area difference of W×2 and wherein W is a variation in the area of the capacitor.

11. A method of fabricating a flat panel display device, comprising:

providing a substrate including a first region in which an organic light emitting diode and a thin film transistor are formed and a second region in which a capacitor is formed;

forming a semiconductor layer on the first region on the substrate;

forming a first capacitor electrode on the second region;

forming a gate insulating layer on the substrate;

forming a gate electrode on the first region on the gate insulating layer, forming a second capacitor electrode on the second region on the gate insulating layer;

injecting a dopant into the semiconductor layer and forming source and drain regions;

forming an interlayer insulating layer on the substrate;

forming first and second contact holes respectively exposing the source and drain regions on the interlayer insulating layer,

forming third and fourth contact holes respectively exposing the first capacitor electrode and the second capacitor electrode;

forming source and drain electrodes connected with the source and drain regions through the first and second contact holes on the first region on the interlayer insulating layer;

forming a first power voltage line connected with the second capacitor electrode through the third contact hole; and

forming a third capacitor electrode connected with the first capacitor electrode through the fourth contact hole and having a different area from the first capacitor electrode on the second region on the interlayer insulating layer.

12. The method according to claim **11**, wherein the first capacitor electrode is formed from the same material as the semiconductor layer.

13. The method according to claim **11**, wherein the second capacitor electrode is formed from the same material as the gate electrode.

14. The method according to claim **11**, wherein the first power voltage line is formed from the same material as the source and drain electrodes.

15. The method according to claim **11**, wherein the third capacitor electrode is formed from the same material as the source and drain electrodes.

16. The method according to claim **11**, wherein the first capacitor electrode is formed in substantially the same layer as the semiconductor layer.

17. The method according to claim **11**, wherein the second capacitor electrode is formed in substantially the same layer as the gate electrode.

18. The method according to claim **11**, wherein the first power voltage line is formed in substantially the same layer as the source and drain electrodes.

19. The method according to claim **11**, wherein the third capacitor electrode is formed in substantially the same layer as the source and drain electrodes.

20. The method according to claim **11**, wherein the first capacitor electrode corresponding to the second capacitor electrode and the third capacitor electrode have an area difference of W×2 and wherein W is a variation in the area of the capacitor.

* * * * *

专利名称(译)	平板显示装置及其制造方法		
公开(公告)号	US20080237585A1	公开(公告)日	2008-10-02
申请号	US12/079720	申请日	2008-03-28
[标]申请(专利权)人(译)	金正日YUN		
申请(专利权)人(译)	金正YUN		
当前申请(专利权)人(译)	金正YUN		
[标]发明人	KIM JONG YUN		
发明人	KIM, JONG-YUN		
IPC分类号	H01L51/00 H01L21/02		
CPC分类号	H01L27/3265 H01L27/1255 H01L28/40 H01L27/3276		
优先权	1020070030478 2007-03-28 KR		
其他公开文献	US7642587		
外部链接	Espacenet USPTO		

摘要(译)

本发明公开了一种平板显示装置，包括具有有机发光二极管和薄膜晶体管的第一区域以及具有电容器的第二区域。电容器包括第一，第二和第三电极，其中第三电容器电极的面积减小，从而确保第一电源电压线和第三电容器电极之间的距离。通过增加第一电容器电极的面积来补偿电容器的总面积。因此，减小了第三电容器电极的面积，同时保持了电容器的总电容，从而防止了由第一电源电压线和第三电容器电极之间的短路引起的暗点。